REMARKS

The above identified patent application has been amended and reconsideration and reexamination are hereby requested.

The Examiner has asked that a drawing be included to facilitate the understanding of the invention.

Applicants have provided a Fig. 1 showing, in a typical digital information processing system, the flow of the divisor/dividend from memory to an arithmetic unit and the flow

of the resulting quotient back to memory. Applicants submit that Fig. 1, and the related accompanying text additions to the Specification on Page 17, is not new matter in that the inherent nature of such a typical digital information processing system and its components are well known in the art (as can be seen or inferred from both the prior art described in the Background of the Invention in the application and in the prior art made of record by the Examiner). As to a specific flow of the steps of the invention showing the producing of the quotient data, since Applicants have provided four detailed examples in the Specification, related drawings reflecting such steps in block diagram form as part of the Figures are considered to be redundant to the understanding of the invention.

The Examiner has brought to Applicants' attention certain informalities in the Specification. In particular, the Examiner has asked Applicants to check to result on Page 10, line 16.

Applicants believe the result on line 16 is correct. The binary number on line 14 represents the decimal sum of: 0 + 0 + 16 + 0 + 0 + 2 + 0 = 18
The binary number on line 15 represents: - (64 + 0 + 0 + 8 + 0 + 0 + 0) = - 72
The binary number on line 16 represents: -(0 + 32 + 16 + 0 + 4 + 2 + 0) = - 54

Applicants have made other corrections accordingly.

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The Examiner has rejected Claims 1 and 2 under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

In particular, the Examiner states, as to Claim 1, that "setting a_i" in steps f and g lacks a proper antecedent basis.

Applicants have amended Claim 1 to call for ... defining a signed-digit partial remainder series R_i where $R_0 = Y$, a first sign series of the partial remainder S_i where $S_0 = 0$, a second sign series of the partial remainder S_{ri}, a quotient bit series a_i, and a counter i beginning from zero...

The Examiner also states, as to Claim 1, that "said" in step k should be deleted.

Applicants have amended Claim 1 to call for ... repeating steps (c) to (j) until i reaches a predetermined value or $R_{i+1} = 0$ ...

The Examiner states, as to Claim 2, that "setting a_i" in steps g and h lacks a proper antecedent basis.

Applicants have amended Claim 2 to call for ... defining a divisor $Y = y_1y_2....y_n$, a dividend $X = x_1x_2....x_s$, a signed-digit partial remainder series R_i where $R_0 = Y$, a first sign series of the partial remainder S_i where $S_0 = 0$, a second sign series of the partial remainder S_{ri}, a quotient bit series a_i, and a counter i beginning from zero ...

The Examiner also states, as to Claim 2, that "said" in step l should be deleted.

Applicants have amended Claim 2 to call for ... repeating steps (d) to (k) until i reaches a predetermined value or $R_{i+1} = 0$ ...

Applicants submit that Claims 1 and 2 particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

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The Examiner has rejected Claims 1 and 2 under 35 USC 101 as being directed to non-statutory subject matter. In particular, the Examiner states that the claims are directed to the preemption of a mathematical algorithm and thus are non-statutory.

Applicants have amended Claim 1 to call for ... In a system for digital information processing, said system having a memory for storing data, a method for generating data representative of a quotient $Q = a_0a_1a_2....a_b$ from data representative of a divisor $Y = y_1y_2....y_n$ and from data representative of a dividend $X = x_1x_2....x_a$, comprising the steps of ... and storing in said memory as said data representative of a quotient, a quotient resulting from step (k).

Applicants have amended Claim 2 to call for ... In a system for digital information processing , said system having a memory for storing data, a method for generating data representative of a signed magnitude quotient $Q_2 = a_sa_0.a_1a_2....a_b$ from data representative of a signed divisor $Y_s = y_s.y_1y_2....y_n$, , and data representative of a signed dividend $X_s = x_s.x_1x_2....x_s$, comprising the steps of ... storing in said memory as said data representative of a quotient, a quotient resulting from step (k).

Newly added Claim 3 calls for ... A system for digital information processing, said system having a memory for storing data, including data representative of a quotient $Q = a_0a_1a_2....a_b$ from data representative of a divisor $Y = y_1y_2....y_n$ and data representative of a dividend $X = x_1x_2....x_a$, said data representative of a quotient generated by a method comprising the steps of ... storing in said memory as said data representative of a quotient, a quotient resulting from step (k).

Newly added Claim 4 calls for ... A system for digital information processing, said system having a memory for storing data, including data of a signed magnitude quotient $Q_2 = a_sa_0.a_1a_2....a_b$ from data representative of a signed divisor $Y_s = y_s.y_1y_2....y_n$, , and data representative of a signed dividend $X_s = x_s.x_1x_2....x_s$, said data representative of a signed magnitude quotient generated by a method comprising the steps of ... storing in said memory as said data representative of a quotient, a quotient resulting from step (l).

Applicants submit that Claims 1 - 4 are directed to statutory subject matter.

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The present invention, as reflected in Claims 1 - 4, provides a method and apparatus for finding a quotient in a digital system. The digital system includes memory for storing data. Binary digital divisor data and binary digital dividend data are processed by digital logic circuit elements in accordance with a series of precise data manipulation steps, which results in binary digital quotient data being produced. The binary digital quotient data is then stored in the memory.

Inherent in such a digital system is that such binary digital divisor data and such binary digital dividend data also stored in memory . Similarly, inherent in such a digital system is that arithmetic logic units perform digital logic manipulation on binary digital data. The arithmetic logic units receive the binary digital data from memory and send binary digital data to memory upon the arithmetic logic unit's completion of their digital logic manipulation. Such a digital system is well recognized as a "machine" under the statutory definition of 35 USC 101.

In a recent CAFC decision, In re Warmerdam, 31 USPQ 2d, 1754 -1760, decided August 1, 1994, patentability under 35 USC 101 was considered. In addition, claim construction, including where a claim was for a machine which incorporates process steps, and where a claim was for a "data structure", was also considered. The court maintained that a patent cannot be obtained for a mathematical algorithm and that the dispositive issue for assessing compliance with S101 is whether the claim is for a process that goes beyond simply manipulating "abstract ideas" or "natural phenomena". The court also maintained that a claim directed to a "data structure" (e.g., A data structure generated by the method of ...) is nothing more than another way of manipulating ideas, stating that the phase "data structure" does not imply a physical arrangement of the contents of a memory. However, the court also addressed a product-by-process claim (e.g., A machine having a memory which contains data representing ... generated by the method of ...) stating that there is no requirement that a claim for a machine which incorporates process steps must conform to the conventional product-by-process claim, recognizing that the storage of data in a memory physically alters the memory and gives rise to a new memory.

Applicants submit that Claims 1 - 4 are directed to statutory subject and are consistent with In re Warmerdam, particularly as to the present invention's physical aspects of storing resulting quotient dat in memory.

In Claim 1, the invention operates in a system for digital information processing. The system includes a memory for storing data. Data representative of a quotient is generated from data representative of a divisor and data representative of a dividend. The data representative of a quotient is stored in the memory of the system. Applicants submits that Claim 1 is for a process that goes beyond simply manipulating "abstract ideas" or "natural phenomena". All data processing involves manipulation of data, including storing results of the manipulation. The process of the present invention, in the context of the digital system in which iit operates, allows for improved, simpler, faster data processing. As such, Applicants submit that a method for generating data representative of a quotient from data representative of a divisor and from data representative of a dividend and storing in memory as data representative of the quotient, a quotient resulting from a certain step in the data manipulation process goes beyond simply manipulating "abstract ideas" or "natural phenomena".

In Claim 2, the invention operates in a system for digital information processing. The system includes a memory for storing data. Data representative of a signed magnitude quotient is generated from data representative of a signed divisor and data representative of a signed dividend. The data representative of a signed magnitude quotient is stored in the memory of the system. As such, the arguments set forth for Claim 1 apply similarly to Claim 2.

In Claim 3, a new machine claim is provided (i.e., the system for digital information processing). The system has a memory for storing data.. Such data includes data representative of a quotient Q from data representative of a divisor and data representative of a dividend. The data representative of a quotient is generated by a method including certain specific steps. On step involves storing in memory as the data representative of a quotient, a quotient resulting from a specific step in the method. Applicants submit that this product by process type claim reflects patentable subject matter, similar to that allowed in In Re Warmerdam, namely a claim for a machine which incorporates process steps not conforming to conventional product-by-process claim, recognizing that the storage of data in a memory physically alters the memory and gives rise to a new memory.

In Claim 4, a new machine claim is provided (i.e., the system for digital information processing). The system has a memory for storing data.. Such data includes data representative of a signed

magnitude quotient from data representative of a signed divisor and data representative of a signed dividend. The data representative of a signed magnitude quotient is generated by a method having certain specific steps. One step includes storing in memory as the data representative of a signed magnitude quotient, a quotient resulting from a specific step in the method. As such, the arguments set forth for Claim 3 apply similarly to Claim 4.

As such, Applicants submit that Claims 1 - 4 are directed to statutory subject matter.

Accordingly, in view of the above amendment and remarks, it is submitted that the claims are patentably distinct over the prior art and that all the rejections to the claims have been overcome. Reconsideration and reexamination of the above Application is requested.

Respectfully submitted,

LADAS & PARRY

By: Richard J. Paciulan

Richard J. Paciulan
Reg. No. 28,248
Attorney for Assignee

Ladas & Parry
5670 Wilshire Boulevard, Suite 2100
Los Angeles, California 90036
(213) 934-2300

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